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#define ETH_CTRL_GET_MAC      1      /* Get the MAC for this device */
#define ETH_CTRL_ADD_MCAST    2      /* Add a multicast address */
#define ETH_CTRL_REMOVE_MCAST 3      /* Remove a multicast address */

/* Ethernet multicast */

#define ETH_NUM_MCAST          32     /* Max multicast addresses */

/* Ethernet NIC type */

#define ETH_TYPE_3C905C        1      /* 3COM 905C */
#define ETH_TYPE_E1000E         2      /* Intel E1000E */
#define ETH_TYPE_QUARK_ETH      3      /* Ethernet on Quark board */

/* Control block for Ethernet device */

struct ethcblk {
    byte state;           /* ETH_STATE_... as defined above */
    struct dentry *phy;   /* physical eth device for Tx DMA */
    byte type;            /* NIC_TYPE_... as defined above */

    /* Pointers to associated structures */

    struct dentry *dev;   /* Address in device switch table */
    void *csr;            /* Control and status register address */
    uint32 pcidev;        /* PCI device number */
    uint32 iobase;         /* I/O base from config */
    uint32 flashbase;     /* Flash base from config */
    uint32 membase;        /* Memory base for device from config */

    void *rxRing;          /* Ptr to array of recv ring descriptors*/
    void *rxBufs;          /* Ptr to Rx packet buffers in memory */
    uint32 rxHead;          /* Index of current head of Rx ring */
    uint32 rxTail;          /* Index of current tail of Rx ring */
    uint32 rxRingSize;      /* Size of Rx ring descriptor array */
    uint32 rxIrq;           /* Count of Rx interrupt requests */

    void *txRing;          /* Ptr to array of xmit ring descriptors*/
    void *txBufs;          /* Ptr to Tx packet buffers in memory */
    uint32 txHead;          /* Index of current head of Tx ring */
    uint32 txTail;          /* Index of current tail of Tx ring */
    uint32 txRingSize;      /* Size of Tx ring descriptor array */
    uint32 txIrq;           /* Count of Tx interrupt requests */

    uint8 devAddress[ETH_ADDR_LEN]; /* MAC address */
}

```